What is claimed is:

1. A semiconductor device comprising:

an SOI substrate having a semiconductor substrate, an insulating layer, and a semiconductor layer of a first conductivity type that are stacked in this order;

element isolation insulating films formed partially in a main surface of said semiconductor layer, with portions of said semiconductor layer interposed between said insulating layer and bottom surfaces of said element isolation insulating films;

a gate structure formed partially on said main surface of said semiconductor layer in an element formation region defined by said element isolation insulating films;

a pair of recesses formed in said element formation region, said recesses being formed in said main surface of said semiconductor layer in portions that are not covered by said gate structure, with a channel formation region under said gate structure interposed between said pair of recesses; and

source/drain regions formed in bottom surfaces of said recesses and having a second conductivity type that is different from said first conductivity type, said source/drain regions forming a pair, with said channel formation region interposed therebetween, and having bottom surfaces or depletion layers that reach said insulating layer.

2. The semiconductor device according to claim 1, wherein the part of said main surface of said semiconductor layer where said gate structure resides forms an angle larger than 90° with a side surface of each said recess.

3. The semiconductor device according to claim 1, wherein each said recess is

positioned beneath said gate structure.

4. The semiconductor device according to claim 1,

wherein said source/drain regions comprise:

first impurity-introduced regions having a relatively low concentration and formed in said main surface of said semiconductor layer; and

second impurity-introduced regions having a relatively high concentration and formed deeper than said first impurity-introduced regions,

wherein a depth from said main surface of said semiconductor layer to said bottom surface of each said recess is smaller than a depth from said main surface of said semiconductor layer to a bottom surface of each said first impurity-introduced region.

5. The semiconductor device according to claim 4,

wherein said source/drain regions further comprise third impurity-introduced regions formed in said main surface of said semiconductor layer, reaching a depth shallower than a depth of said second impurity-introduced regions.

6. The semiconductor device according to claim 1,

wherein said source/drain regions comprise:

first impurity-introduced regions having a relatively low concentration and formed in said main surface of said semiconductor layer;

second impurity-introduced regions having a relatively high concentration and formed deeper than said first impurity-introduced regions; and

third impurity-introduced regions formed in said main surface of said semiconductor layer,

wherein a depth from said main surface of said semiconductor layer to bottom surfaces of said third impurity-introduced regions is greater than a depth from said main surface of said semiconductor layer to bottom surfaces of said first impurity-introduced regions, and

wherein a depth from said main surface of said semiconductor layer to said bottom surfaces of said recesses is smaller than a depth from said main surface of said semiconductor layer to said bottom surfaces of said third impurity-introduced regions.

7. The semiconductor device according to claim 1,

wherein said gate structure comprises:

a gate insulating film formed on said main surface of said semiconductor layer;

a gate electrode formed on said gate insulating film; and

first sidewalls formed on sides of said gate electrode;

and wherein said semiconductor device further comprises:

second sidewalls formed on said bottom surfaces of said recesses and in contact with said first sidewalls; and

metal-semiconductor compound layers formed on said source/drain regions in portions that are not covered by said second sidewalls.

8. The semiconductor device according to claim 7, further comprising third sidewalls formed on said bottom surfaces of said recesses and being in contact with said element isolation insulating films,

wherein said metal-semiconductor compound layers are formed on said source/drain regions in portions that are not covered by said second and third sidewalls.

9. The semiconductor device according to claim 1, further comprising:

semiconductor regions formed on the bottom surfaces of said recesses; and

metal-semiconductor compound layers formed on said semiconductor regions.

10. The semiconductor device according to claim 1,

wherein said SOI substrate comprises an NMOS transistor and a PMOS transistor that are formed therein, and

said semiconductor device is said NMOS transistor or said PMOS transistor.

11. The semiconductor device according to claim 1,

wherein said SOI substrate comprises a first transistor operating at a relatively low power-supply voltage and a second transistor operating at a relatively high power-supply voltage; and

said semiconductor device is said first transistor or said second transistor.